

What is claimed is:

- 5 1. A codec comprising a programmed digital signal processor and an accelerator core in which computation of a coding algorithm is divided between the digital signal processor and the accelerator core, computationally relatively intensive parts of a coding algorithm being performed by the accelerator core.
2. A codec according to claim 1 in which the accelerator core includes a processor structure that is capable of processing multiple items of data simultaneously.
- 10 3. A codec according to claim 2 in which the processor is a vector processor.
4. A codec according to claim 2 in which the processor structure has a single-instruction multiple-data architecture.
5. A codec according to claim 2 in which the processor structure has an instruction set that is optimised to perform encoding to a predetermined standard.
- 15 6. A codec according to claim 5 in which the instruction set is optimised to perform CELP coding of speech signals.
7. A codec according to claim 1 in which the accelerator core has includes a plurality of similar operational units capable of carrying out simultaneous data processing operations.
- 20 8. A codec according to claim 7 in which an operation can be assigned for performance by one or more of the operational units on a plurality of data elements.
9. A codec according to claim 8 in which the number of operational units that perform a given operation can be determined under programmatical control.

10. A codec according to claim 7 including a register bank, the operational units performing operations on data stored in the register bank.
11. A codec according to claim 7 in which each operational unit can perform operations upon the output of one or more of the operational units.
- 5 12. A codec according to claim 7 in which each operational unit can store the result of an operation in the register bank.
13. A codec according to claim 7 in which an operation can be performed on the outputs of a plurality of the operational units to derive a further output value.
- 10 14. A codec according to claim 13 in which the outputs of a plurality of the operational units can be summed.
15. A codec according to claim 7 in which each operational unit can access a common memory unit.
16. A codec according to claim 15 in which the common memory unit includes a ROM.
- 15 17. A codec according to claim 15 in which the common memory unit includes a RAM.
18. A codec according to claim 7 in which each operational unit is a MAC unit.
19. A codec according to claim 1 in which the accelerator core is operative to execute program instructions as a vector processor.
- 20 20. A codec according to claim 19 in which the program instructions are executed as microcode.
21. A codec according to claim 19 including a decoder by means of which the program instructions are decoded for execution by one or more operational units.

22. A codec according to claim 21 in which the decoder includes a finite state machine.

23. A codec according to claim 21 in which the decoder includes a programmed memory device.

5 24. A computer program product for defining a codec, the codec comprising a programmed digital signal processor and an accelerator core in which computation of a coding algorithm is divided between the digital signal processor and the accelerator core, computationally relatively intensive parts of a coding algorithm being performed by the accelerator core.

10 25. A computer program product according to claim 24 expressed in a hardware definition language.